The Performance Comparison of CMOS Vs Biploar VCO In SiGe BiCMOS technology

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Abstract — **Two 2.3 GHz VCO monolithic ICs using CMOS and bipolar topology respectively for WCDMA transmitter application are designed and fabricated in IBM 0.25 μm SiGe BiCMOS technology. The design trade-offs of each design topology are discussed. The results indicated that the CMOS version has better phase noise, more power efficient, but more sensitive to temperature and process than that of bipolar counter partner.**

I. INTRODUCTION

Voltage controlled oscillator (VCO) is one of the critical circuit blocks for wireless handset applications. There has been an increasing trend to implement VCO on chip in CMOS or BiCMOS technology for highly integrated transceiver in order to reduce cost and size. Although Bipolar VCO has performed very well [1-3], the performance of CMOS VCO [4-6] has steadily improved, even catching up over last few years. It is of a lot of interest to compare the design tradeoffs and the performance difference of these two different topology VCO designs. BiCMOS is an excellent technology to use for such a comparison, since it offers a full suite of bipolar and CMOS transistors as well as high performance passive devices. In this paper, we present the work of two VCO designs for the same electrical specifications targeted for WCDMA transmitter application with implementations in CMOS and bipolar topology, respectively. The system configuration and the circuit design for each design is discussed in detail, followed by the performance comparison of the tested results.

II. SYSTEM CONFIGURATION & CIRCUIT DESIGN

One of the key VCO specifications in this study is to achieve a phase noise of −100 dBc/Hz at 100KHz offset with a center frequency of 2.3GHz. As a circuit block for WCDMA transmitter chipset, the design requires enough margins for temperature, supply and process variation. There are two system configurations considered, shown on Fig.1 (A) and Fig. 1 (B). The first

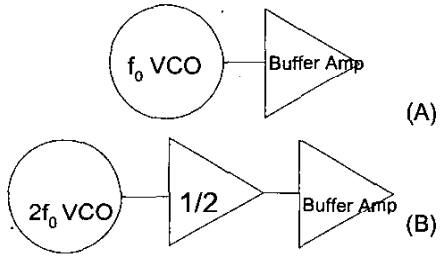

Fig.1 Block diagram of two VCO system configurations

one is to design the VCO directly in the fundamental frequency (f_0=2.3 GHz). The second one is to design it at twice the frequency ($2f_0$ =4.6 GHz) and follow with a divide-by-2 circuit. Theoretically, when operating at a lower frequency, the noise contribution from the active device will be lower and will result in lower phase noise, assumed that the quality factor of the tank is the same. However, in a fully integrated VCO design, the phase noise is usually limited by the quality factor of the tank inductor. Therefore, a VCO operating at doubled frequency and then dividing down can have a better phase noise because the benefit from the improvement of the quality factor is more than the added noise contribution from the active devices. The other benefit is that the chip area can be smaller when the VCO is operating at higher frequency due to smaller reactance of the tank inductance and capacitance required. In addition, the tradeoffs among the tank impedance, current consumption and allowable voltage swing will aid in decision on what topology to be used.

Theoretical analysis and simulation results show that it is preferred to design a CMOS VCO at the fundamental frequency directly because it allows a larger voltage swing and a large tank inductor with a relative good quality factor. A bipolar VCO operating at twice the fundamental frequency ($2f_0$) has better overall performance because its phase noise performance is more dependent on good quality factor of the tank and

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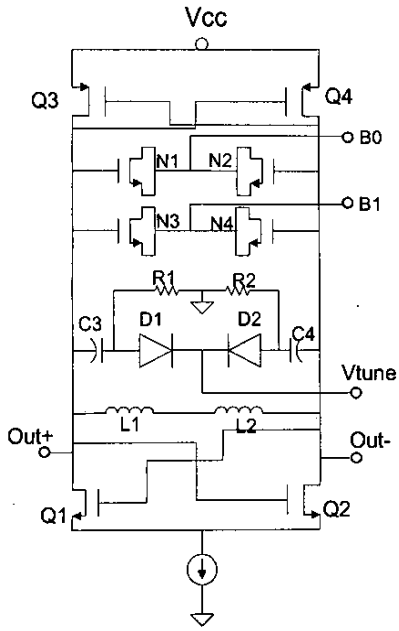

Fig.2. CMOS version of VCO using CMOS as active device

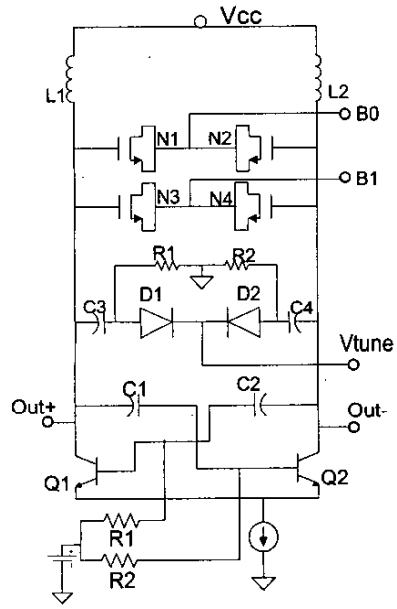

Fig.3. Bipolar version of VCO using BJT as active device

its voltage swing is limited by the PN junctions of the transistors. Although a divide-by-2 circuit consumes little current in bipolar VCO, it adds the benefit of improved load pull effect.

Both configurations of VCO are designed in IBM 0.25 μm SiGe BiCMOS technology. As shown on Fig. 2 and Fig. 3, both VCO core circuits use fully differential cross-coupled topology. The key difference is on the active devices that generate negative gm. Although 1/f noise is much larger in CMOS devices than that of silicon or SiGe bipolar devices, its effect on VCO phase noise can be minimized by using both NMOS (Q1 and Q2) and PMOS (Q3 and Q4), seen in Fig, 2. By properly sizing CMOS devices and the ratio between NMOS and PMOS transistors, the degradation in phase noise due to 1/f noise can be significantly reduced [4]. Another way to reduce 1/f noise is to increase sizes of all CMOS devices, as the larger the CMOS device is, the smaller the 1/f noise is. However, too large CMOS devices can lead to too much fix parasitic capacitance. Thus it would reduce the frequency tuning range of VCO. Only current biasing is needed and the sizes of both NMOS and PMOS directly affect the biasing current.

For bipolar VCO, Hetero-junction Bipolar Transistors (HBT) Q1 and Q2 are used as a negative gm generator, shown in Fig.3. Two capacitors C1 and C2 are used to control the coupling strength of the positive feedback. They also serve the purpose of decoupling the DC voltage biasing at the bases from the collector RF signal. There are both current tail biasing as well as voltage biasing. Base voltages are provided by a voltage source through two resistors R1 and R2.

In both configurations, similar tuning circuitry is used to ease the comparison of the performances. In order to widen the total tuning bandwidth, digital tuning is used in conjunction with analog tuning. Varactor D1 and D2 are base to collector junction capacitors for analog tuning. Capacitor C3 and C4 are used to decouple the varactors from the voltage supply to improve the supply push performance. CMOS transistors N1 to N4 are used as digital varactors to provide the digital band switching to extend the total frequency coverage. When VCO with digital band switching is used in a frequency synthesizer, an automatically band switching circuit is typically needed to make the band switching process seamless in the system [2].

In IBM 0.25 μm SiGe BiCMOS process, the bipolar and CMOS have comparable *ft* with 48GHz for the bipolar and 40GHz for the CMOS. Thus CMOS VCO will have the advantage of larger gain due to the gm contributions from both PMOS and NMOS. The higher gain of CMOS VCO will result in less current consumption.

In bipolar VCO, the voltage swing is limited by the saturation condition of the bipolar transistors Q1 and Q2. However, in CMOS VCO, the voltage swing is limited by the CMOS gate breakdown voltage, which allows a much larger swing in CMOS VCO over the bipolar version. In order to avoid forward biasing varactor diodes D1, and D2, a trade-off needs to be made between the voltage swing in the tank and the tuning bandwidth by adjusting capacitors C3 and C4.

The divide-by-2 circuit is made of two flip-flops. With about 1 mA, its noise floor can reach -155 dBm/Hz or less. So up to 10MHz offset, the VCO core itself determines the phase noise of VCO.

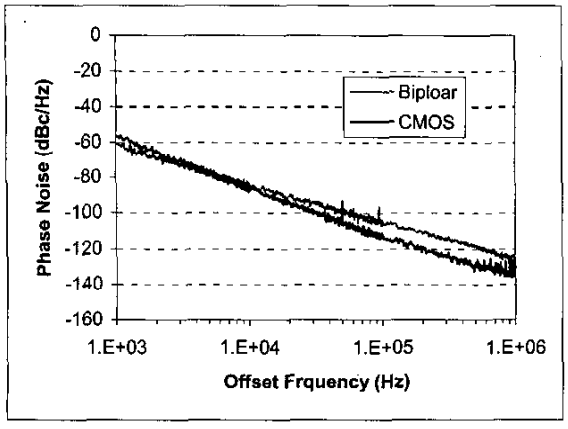

Fig 4. Phase noise comparison of CMOS and bipolar VCO

III. Measured Performance

In order to minimize the process effect, both CMOS and bipolar VCO designs are run together on the same wafer. Both chips are packaged in QFN20 for evaluation. The tests are performed using Aeroflex PN9000 Phase Noise Test System. The phase noise results at 2.3GHz center frequency are compared in Fig. 4 for CMOS and bipolar VCOs. As shown in Fig.4, the close in phase noise of the bipolar VCO is better than that of the CMOS VCO but it is worse than that of the CMOS VCO at higher frequency offsets. While both VCOs meet the required phase noise specs at 100KHz offset, CMOS VCO achieves 8 dB better phase noise than that of bipolar one. The corner frequency of the 1/f noise in the CMOS VCO is around 100KHz.

With 3V supply voltage, CMOS and bipolar VCO consumes 4.5mA and 5.2 mA, respectively. Bipolar VCO current includes 1 mA current from the divide-by-2 circuit. Excluding the bond pads, CMOS VCO has a slightly smaller chip size (500um x 600um) than that of bipolar version (800um x 600um). The larger size in bipolar version is mainly due to the custom high quality inductors and the divide-by-2 circuit.

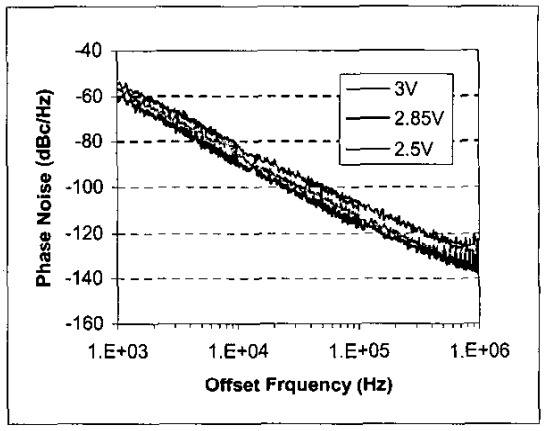

Fig 5. CMOS Phase Noise vs. Supply voltage

The frequency sensitivity to supply voltage is similar for both CMOS and bipolar VCOs. The measured supply push is about the same (2 MHz per 0.1V supply voltage change). The phase noise sensitivity to temperature and supply for the two VCOs is different. For CMOS VCO, as seen in Fig. 5, the phase noise improved initially when voltage decreases from 3V to 2.85V. The phase noise degrades significantly when the supply drops to 2.5V, but it still meets the specification. This sensitivity mainly originates from the biasing scheme used in CMOS VCO. Because the current is self-biased by NMOS and PMOS transistors, its biasing current and phase noise is very sensitive to supply voltage, temperature and process variations. Although a current source can be added to stabilize the biasing current and reduce the sensitivity, the current source will degrade the phase noise in a considerable amount and its influence to the phase noise can be filtered out effectively only by using off-chip inductor and capacitors. The simplicity of CMOS VCO biasing eliminates the noise contribution from a separate biasing circuit. This is one of the reasons that the phase noise of the CMOS VCO can outperform the bipolar one.

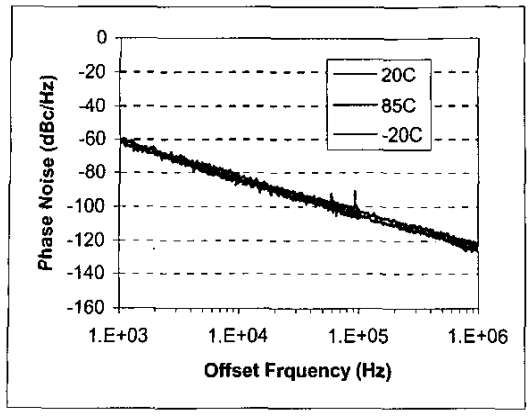

Fig 6. Bipolar Phase Noise vs. Temperature

The phase noise of bipolar VCO is less sensitive to the supply voltage, temperature than that of CMOS one. For bipolar VCO, its phase noise changes less than +/- 1dB over the supply voltage rang of 3 +/- 0.15V. The phase noise changes less than +/- 1.5dB over the temperature range of –20C to 85C, as shown in Fig. 6. Although there is no process spread data of both VCOs, simulations over corners indicate that bipolar VCO is much more robust over process and temperature than that of CMOS one, so less margin is necessary for nominal design in bipolar VCO.

V. CONCLUSION

Targeted for WCDMA transmitter application, CMOS and bipolar VCO in IBM SiGe technology are designed and tested. The performances of VCO designs in CMOS and bipolar topologies are compared. CMOS version has exceeded the performance of bipolar one, both in terms of power efficiency for the phase noise and chip area. Bipolar version is less sensitive to the process and temperature.

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